In the claims

This listing of claims will replace all prior versions, and listings of claims, in the application:

1-8. (Cancelled)

9. (Previously presented) A method for fabricating a semiconductor substrate comprising:

a) formation of a multiplicity of depressions and a capacitor counterelectrode in a carrier substrate;

b) formation of a dielectric layer at a surface of the depressions and of the carrier substrate;

c) formation and patterning of an electrically conductive layer on the dielectric layer for realizing a multiplicity of capacitor electrodes at least in the multiplicity of depressions;

d) formation of a first insulation partial layer at the processed surface of the carrier substrate;

e) provision of a semiconductor component substrate with a splitting-off boundary layer, and a second insulation partial layer;

f) connection of the semiconductor component substrate and the carrier substrate at their insulating partial layers to form an insulation layer; and

g) splitting off part of the semiconductor component substrate at the splitting-off boundary layer.

10. (Previously presented) The method as claimed in claim 9, wherein, in step a),

a1) an electrochemical pore etching is carried out for forming as depressions in the semiconductor substrate; and

a2) a doping of the semiconductor substrate is carried out in the vicinity of the pores for forming a further electrically conductive layer as capacitor counterelectrode.

11. (Previously presented) The method as claimed in 10, wherein, in step a2),

a21) a formation of a doping glass is carried out at least in the pores;

a22) a thermal treatment is carried out; and

a23) a wet-chemical removal of the doping glass is carried out.

12. (Currently amended) The method as claimed in claim 9, wherein, in step b), a high-temperature-resistant capacitor dielectric with a high dielectric constant is formed over ~~the~~ a whole area of the surface of the depressions and of the carrier substrate.

13. (Previously presented) The method as claimed in patent claim 12, wherein at least one of nitrided oxide, Al_2O_3 and TiO_2 is formed as the capacitor dielectric.

14. (Currently amended) The method as claimed in claim 9, wherein, in step c),

c1) the electrically conductive layer is formed for filling the depressions over ~~the~~ a whole area of the dielectric layer; and

c2) the electronically conductive layer is at least partially or completely removed as far as the dielectric layer at the surface of the carrier substrate.

15. (Previously presented) The method as claimed in patent claim 14, wherein,

in step c1), in-situ-doped polysilicon is deposited; and

in step c2), photolithographic patterning with an isotropic etching-back is carried out in such a way that a multiplicity of capacitor electrodes are connected to one another for realizing a group capacitor.

16. (Previously presented) The method as claimed in claim 9, wherein in step d), a TEOS deposition method is carried out.

17. (Previously presented) The method as claimed in claim 9, wherein in step e), a semiconductor wafer with an oxide layer (2B) is provided, the splitting-off boundary layer being formed by means of hydrogen implantation.

18. (Previously presented) The method as claimed in claim 9, wherein in step f), the connection is carried out by means of wafer bonding.

19. (Previously presented) The method as claimed in claim 9, wherein in step g), the splitting off is carried out by means of a further thermal treatment.

20-24. (Cancelled)

25. (Previously presented) A method for fabricating a DRAM memory cell in a semiconductor substrate, the method comprising:

a) fabrication of the semiconductor substrate including:

a0) formation of a multiplicity of depressions and a capacitor counterelectrode in the semiconductor substrate;

b0) formation of a dielectric layer at a surface of the depressions and of the semiconductor substrate;

c0) formation and patterning of an electrically conductive layer on the dielectric layer for realizing a multiplicity of capacitor electrodes at least in the multiplicity of depressions;

d0) formation of a first insulation partial layer at the processed surface of the semiconductor substrate;

e0) provision of a semiconductor component substrate with a splitting-off boundary layer, and a second insulation partial layer;

f0) connection of the semiconductor component substrate and the semiconductor substrate at their insulating partial layers to form an insulation layer; and

g0) splitting off part of the semiconductor component substrate at the splitting-off boundary layer to form a semiconductor component layer,

the method further comprising:

b) formation of a shallow trench isolation in the semiconductor component layer for realizing active regions;

c) formation of a selection transistor having source/drain regions, a gate dielectric, a control layer serving as wordline and a gate insulation;

d) formation of a contact hole at least in the insulation layer and the semiconductor component layer;

e) formation of a connecting layer in the contact hole between a source/drain region of the selection transistor and at least one capacitor electrode;

f) formation of an intermediate insulation layer with a bitline contact to a complementary source/drain region; and

g) formation and patterning of a bitline layer for realizing a bitline at the surface of the intermediate insulation layer.

26. (Previously presented) The method as claimed in claim 25, wherein in step d) the contact hole is etched free in a self-aligning manner using the gate insulation and a lithographic method.

27. (Previously presented) The method as claimed in claim 25, wherein in step e) to form the connecting layer, a further in-situ-doped polycrystalline semiconductor layer is deposited over the whole area of the semiconductor substrate and subsequently etched back isotropically or anisotropically.